I claim:

1. A method for forming a structure element in a layer arranged on a wafer by a first mask and a second trimming mask assigned to the first mask, comprising:

providing the wafer with the layer, the first mask, and the second trimming mask;

applying a first photosensitive resist layer to the layer;

projecting a first mask structure pattern arranged on the first mask into the first resist layer to form an exposed resist structure, the exposed resist structure at least partly surrounding an unexposed resist element;

developing the first resist layer;

etching the layer with a transfer of the exposed resist structure into the layer, thereby forming an elevated structure element in the layer below the unexposed resist element;

removing the first resist layer;

applying a second photosensitive resist layer to the layer;

projecting a second mask structure pattern arranged on the second trimming mask into the second resist layer to form a second exposed resist structure in the second resist layer, the second exposed resist structure at least partly covering the elevated structure element in the layer;

developing the second resist layer; and

etching the layer with a transfer of the second exposed resist structure into the layer and the elevated structure element.

2. The method as claimed in claim 1, wherein projecting the first mask

structure pattern arranged on the first mask is carried out using an alternating or a chromeless phase mask.

3. The method as claimed in claim 1, wherein projecting the first mask structure pattern arranged on the first mask is carried out using a chrome or halftone phase mask with oblique exposure.

4. The method as claimed in claim 1, wherein the elevated structure element is formed in the layer, the elevated structure element including an electrically conductive material.

5. The method as claimed in claim 1, wherein projecting the first mask structure pattern arranged on the first mask forms a plurality of elevated metal interconnects, the metal interconnects being arranged substantially parallel.

6. The method as claimed in claim 5, wherein, in etching of the layer with a transfer of the second exposed resist structure into the layer, at least one of the elevated metal interconnects is separated into at least two structure elements.

7. The method as claimed in claim 1, wherein projecting the first mask structure pattern arranged on the first mask forms the elevated structure element in a partial region by a phase jump and sets up on the first mask between two adjoining transparent regions on the first mask, and etching of the layer with a transfer of the second exposed resist structure into the layer removes the partial region.

8. The method as claimed in claim 1, wherein, between removing the first resist layer and applying the second photosensitive resist layer, an intermediate layer is deposited and patterned lithographically.

9. The method as claimed in claim 8, wherein an electrically insulating material is used as material of the intermediate layer.

10. The method as claimed in claim 8, wherein, in the lithographic patterning of the intermediate layer, the elevated structure element is uncovered below the intermediate layer by removal of a part of the intermediate layer.

11. The method as claimed in claim 10, wherein, in projecting the second mask structure pattern arranged on the second trimming mask into the second resist layer, a third exposed resist structure is exposed in the second resist layer, the third exposed resist structure covering a region above the intermediate layer which has not been previously removed during the lithographic patterning.

12. The method as claimed in claim 11, wherein the third exposed resist structure for forming a contact hole, is transferred into the intermediate layer, the contact hole being filled with an electrically conductive material in a further step.

13. The method as claimed in claim 2, wherein projecting the first mask structure pattern arranged on the first mask forms a plurality of elevated metal interconnects, the metal interconnects being arranged substantially parallel.

14. The method as claimed in claim 3, wherein projecting the first mask structure pattern arranged on the first mask forms a plurality of elevated metal interconnects, the metal interconnects being arranged substantially parallel.

15. The method as claimed in claim 13, wherein, in etching of the layer with a transfer of the second exposed resist structure into the layer, at least one of the elevated metal interconnects is separated into at least two structure elements.

16. The method as claimed in claim 14, wherein, in etching of the layer with a transfer of the second exposed resist structure into the layer, at least one of the elevated metal interconnects is separated into at least two structure elements.